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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	Total Pages: 38
First Named Inventor or Application Identifier	KENNETH MEADE LAKIN
Express Mail Label No.	EI267046469US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 15]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets 3]
4. Oath or Declaration [Total Pages 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet & document(s))
9. [X] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [X] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: _____

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____ / _____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

NAME	G. Joseph Buck				
ADDRESS	3868 Carson St., Ste. 315				
CITY	Torrance	STATE	CA	ZIP CODE	90503
COUNTRY	USA	TELEPHONE	(310) 540-8840	FAX	

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CERTIFICATE OF MAILING BY EXPRESS MAIL

In Re: Patent application of Lakin, Rose and McCarron
for: Chip-Scale Electronic Component Package

I hereby certify that this correspondence, which conrrespondence consists of:

1) Utility Patent Application Transmittal;
2) Fee Transmittal and check no. 591 for $435.00;
3) Specification;
4) Drawings - 3 sheets;
5) Declaration - 3 pages;
6) 2 - statements claiming small entity status;
7) Certificate under 37 C.F.R. 3.73(b) (with 3 pages attached);
8) Recordation form;
9) 3 pages of assignments of one property
10) Postcard acknowledging receipt;
11) The within certificate of mailing;

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Washington D.C. 20231

on July 14, 1998.

G. Joseph Buck
Registration No. 29,519

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FEE TRANSMITTAL

Note Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 435.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Lakin
Group Art Unit	
Examiner Name	
Attorney Docket Number	

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number
Deposit Account Name

☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed: Check No.0951
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	395.00
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 395.00

2. CLAIMS

		Extra		Fee from below		Fee Paid
Total Claims	12 -20 =	0	X		=	
Independent Claims	2 - 3 =	0	X		=	
Multiple Dependent Claims		0	X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	G. Joseph Buck			Reg. Number	29,519
Signature		Date	7/14/98	Deposit Account User ID	

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CHIP-SCALE ELECTRONIC COMPONENT PACKAGE

The invention described herein was made under or in the course of a contract with the U.S. Government.

1. Background of the Invention

a. Field of the Invention

This invention pertains to the packaging of electronic components and devices such as integrated circuit chips within chip-scale sized packages. More particularly this invention pertains to the packaging of acoustic wave devices and related components.

b. Description of the Prior Art

The development of very small electronic components and devices such as semi-conductor integrated circuits has given rise to the need for packages adapted for use with such small components and devices. Such packages typically must hold in place and contain such components and protect the components from harm from the environment, e.g. damage from mechanical contact, harmful electrical contact, and contact with harmful liquids and gases. The packages also usually must provide electrical connections to the components within the packages. Devices for high frequency operation must also be packaged such that the electrical connections to the device do not introduce detrimental parasitic effects.

A widely used, prior art package consists simply of the encapsulation of the integrated circuit chip, or die, within a plastic block of material, e.g. the ubiquitous rectangular solid block of plastic (dual in-line package "DIP") that has 14 or more external pins located along two sides of the block and contains a chip holding from 256 thousand to 256 million bits of random access memory. Typically, the integrated circuit chip is placed upon a lead frame and bond wires are connected between the chip and the lead frame. The chip and lead frame are then encapsulated in plastic. An alternate method of packaging is to place the die into a package having existing walls, sides and leads, connecting bond wires between the die and package lead pads and then attaching a lid to the package. Such packages, however, are unsuitable for use at microwave frequencies because the wire bond lead lengths give rise to excessive inductances and other parasitic effects that degrade device performance.

Surface acoustic wave devices and related devices such as thin film bulk-wave resonators have been developed for use with integrated circuit devices. The dice upon which these surface acoustic wave devices and resonators are fabricated typically are "chip-scale" in size, having dimensions of the order of a few millimeters in length and width and thicknesses of the order of one-quarter of a millimeter. Such chip-scale devices, however, cannot be packaged using the encapsulation technique described above, because the portion of the surface of the die that supports acoustic waves or the portion of the die that acts as an acoustic resonator must be free to deform or vibrate. If such acoustic

devices were encapsulated, the portion of the die that supported the acoustic waves or that supported acoustic deformations or vibrations would be unable to deform or vibrate and the device would then be inoperable.

In a paper titled "A New All Quartz Package for SAW Devices", in the 39th Annual Frequency Control Symposium - 1985, p. 519, Parker, Callerame and Montress disclose a package for a surface acoustic wave ("SAW") device that utilizes a quartz lid placed upon top of the substrate that contains the device, which lid is bonded to the substrate using a glass frit that provides a hermetic seal and offsets the lid from the acoustically active surface of the substrate. The electrical connections to the acoustic device, however are made via conductors located on the substrate that pass through, or under the glass frit. The quartz lid does not include electrical connections to the acoustic device. As a consequence, the packaging device described by Parker et al, is not adapted for surface mounting to a printed circuit board.

2. Summary of the Invention

The present invention is a compact package for such chip-scale acoustic wave and resonator devices, which package protects the device from damage, provides electrical connections to the device and provides a space within which the portion of the die that supports acoustic waves or acoustically deforms or vibrates

is free to acoustically deform or vibrate. The present invention utilizes the die, upon which the acoustic device is fabricated, as part of the package.

3. Brief Description of the Drawings

Figure 1 is an exploded, pictorial view of the preferred embodiment of the invention. Figures 2A, 2B and 2C are respectively top, front and bottom views of the lid portion of this invention. Figure 3A is a front view of the referred embodiment showing the lid attached to the die and figure 3B is a cross-sectional, front view of the invention.

4. Detailed Description

Referring to figure 1, a chip, or die 1 of alumina, sapphire or other suitable material, includes at its upper surface 3 an acoustic surface wave device, resonator, or other acoustic device 2. Typically a large number of acoustic devices are fabricated at one time on a single wafer of sapphire or other suitable material by etching away portions of the wafer and/or depositing successive layers of material upon the wafer and then etching away portions of the deposited materials. The wafer is then cut into individual dice, each die containing one or more acoustic devices. Each die typically may have a length and width of the order of 1 to 5 millimeters and a thickness of the order of one-quarter to one-half of a millimeter.

Die 1 typically will include one or more electrical signal connectors pads 4 on its upper surface 3 for the input and output of electrical signals to device 2. In the preferred embodiment, die 1 includes a bonding strip 5, which is an electrically conducting strip on the upper surface 3 of die 1 that surrounds acoustic device 2. In the preferred embodiment, bonding strip 5 operates as an electrical ground and a counterpoise for the input and output of electrical signals to and from electrical signal connector pads 4.

As depicted in figure 1, the preferred embodiment of this invention includes a lid 6 made of alumina, sapphire or other suitable material having a length and width substantially similar to the length and width of die 1 and having a thickness typically of the order of one-quarter of a millimeter. As depicted in fig. 1 and in fig. 2C, in the preferred embodiment, lid 6 includes on its lower surface 7 an electrically conducting bonding strip 8 that is similar in shape and position to bonding strip 5 on die 1.

In figure 1, lid 6 is depicted in an "exploded" position relative to die 1. As shown in fig. 3A and fig. 3B, lid 6 actually is adjacent to and bonded to die 1. Referring to figs. 3A and 3B, bonding strip 5 on die 1 and bonding strip 8 on lid 6 are joined together in the package of this invention by a thin layer of bonding material 9. In the preferred embodiment, the bonding material is a gold/tin alloy having a melting point of approximately 280 degrees. The alloy is electrically conductive and electrically connects bonding strip 5 to bonding strip 8. In

the preferred embodiment, bonding strips 5 and 8 completely surround device 2 and the bonding together of these two strips hermetically seals device 2 from the environment. The thickness of the thin layer of bonding material 9, together with the thicknesses of bonding strip 5 and bonding strip 8, provide sufficient free space 15 above surface 3 of die 1 such that the portions of device 2 that deform acoustically or vibrate do not contact lid 6 and are free to deform acoustically or to vibrate as required for the proper operation of the device.

Referring to figs. 2A, 2B, and 2C, in the preferred embodiment, lid 6 includes on its upper surface 9, an electrical conducting strip 10 and includes electrically conducting pads that form upper surface signal connector pads 11 that provide electrical connections for the input of signals to and the output of signals from the device contained within the package of this invention. Lid 6 includes on its lower surface 7 electrically conducting signal connector pads that are located under the upper surface signal connector pads 11 and that form lower surface signal connector pads 12. Lid 6 includes holes 13 passing from its upper surface 9 to its bottom surface 7. Lasers or other means may be used to fabricate the holes. Holes 13 are either lined or filled with an electrically conductive material so as to connect electrically conducting strip 10 to strip 8 and to connect electrically the upper surface signal connector pads 11 to the respective lower surface signal connector pads 12. The entire package of this invention may then be attached, lid side down, to a printed circuit by inverting the package and soldering

conducting strips 10 and upper input and output connectors 11 onto the printed circuit board so as to bond and connect the package physically and electrically to the printed circuit board.

Instead of soldering the entire areas of bonding strip 10 and signal connector pads 11 to the printed circuit board, a grid of high temperature solder balls may be used to attach, and electrically connect, the package to the printed circuit board.

It should be understood that although strips 10 and strips 5 and 8 have been described as conducting, in other embodiments where a ground or counterpoise for the balanced or unbalance input and output of electrical signals to and from the device is provided by other electrical connections to device 2, bonding strip 5 need not, in fact, be used as a signal ground or counterpoise, but, instead, may be used simply to provide a surface to which lid 6 is bonded. Similarly, bonding strips 8 and 10 need not be conductors, and need not be grounded.

Although in the preferred embodiment the bonding together of strip 5 and strip 8 hermetically seals the device, in instances where the device need not be hermetically sealed, strip 5 and strip 8 need not completely encompass, nor hermetically seal, the device.

Furthermore, although the preferred embodiment includes connectors for both the input and output of electrical signals

from the electronic device, this invention can be used as a package for a single port device.

It should also be understood that the package of this invention can be used to package an acoustic wave device which has active acoustic regions on both the upper and lower surfaces of the die on which, or in which, the device is fabricated, simply by attaching a first lid to the upper surface of the die the in the manner of this invention, and attaching a second lid to the lower surface of the die in the same manner.

5. Claims

We claim:

1

a chip-scale package for an electronic device of the type having an acoustically active portion comprising:

a die having an upper surface and having at least one electronic device located at the upper surface of the die and having a plurality of signal connector pads located upon the upper surface of the die and having a bonding strip located upon the upper surface of the die,

a lid made of a substantially non-conducting material and having a lower surface and an upper surface and having a lower

surface bonding strip and a plurality of lower surface signal connector pads located upon the lower surface of the lid and having a plurality of upper surface signal connector pads located upon the upper surface of the lid, each upper surface signal connector pad being electrically connected to a lower surface signal connector pad,

each lower surface signal connector pad on the lid being electrically connected to a signal connector pad located upon the upper surface of the die,

the bonding strip located upon the upper surface of the die being bonded by a bonding material to the bonding strip located upon the lower surface of the lid, the lid covering the electronic device but not being in physical contact with the acoustically active portion of the electronic device.

2

The package of claim 1 wherein each upper surface signal connector pad is electrically connected to a lower surface signal connector pad by means of conducting material located within a hole in the substantially non-conducting material of the lid, which hole connects the upper surface of the lid to the lower surface of the lid.

3

The package of claim 1 wherein the bonding strip on the upper surface of the die and the bonding strip on the lower surface of the lid are made of conducting material and are electrically connected by the bonding material, the lid further including a conducting strip on the upper surface of the lid that is electrically connected to the bonding strip on the lower surface of the lid.

4

The package of claim 2 wherein the bonding strip on the upper surface of the die and the bonding strip on the lower surface of the lid are made of conducting material and are electrically connected by the bonding material, the lid further including a conducting strip on the upper surface of the lid that is electrically connected to the bonding strip on the lower surface of the lid by means of conducting material located within a hole in the substantially non-conducting material of the lid, which hole connects the upper surface of the lid to the lower surface of the lid.

5

The package of claim 2 in which the conducting strip on the upper surface of the lid and the bonding strip on the lower

surface of the lid and the bonding strip on the upper surface of the die act as a signal ground.

6

The package of claim 4 in which the conducting strip on the upper surface of the lid and the bonding strip on the lower surface of the lid and the bonding strip on the upper surface of the die act as a signal ground.

7

The package of claim 1 in which the bonding strip on the upper surface of the die and the bonding strip on the lower surface of the lid completely surround the acoustically active portion of the electronic device and are bonded together so as to seal the electronic device hermetically.

8

The package of claim 2 in which the bonding strip on the upper surface of the die and the bonding strip on the lower surface of the lid completely surround the acoustically active portion of the electronic device and are bonded together so as to seal the electronic device hermetically.

9

The package of claim 4 in which the bonding strip on the upper surface of the die and the bonding strip on the lower surface of the lid completely surround the acoustically active portion of the electronic device and are bonded together so as to seal the electronic device hermetically.

10

The package of claim 6 in which the bonding strip on the upper surface of the die and the bonding strip on the lower surface of the lid completely surround the acoustically active portion of the electronic device and are bonded together so as to seal the electronic device hermetically.

11

A chip-scale package for an electronic device of the type having an acoustically active portion comprising:

a die having an upper surface and having at least one electronic device located at the upper surface of the die and having a signal connector pad located upon the upper surface of the die and having a bonding strip located upon the upper surface of the die,

12

a lid made of a substantially non-conducting material and having a lower surface and an upper surface and having a lower surface bonding strip and a lower surface signal connector pad located upon the lower surface of the lid and having an upper surface signal connector pad located upon the upper surface of the lid, the upper surface signal connector pad being electrically connected to the lower surface signal connector pad,

the lower surface signal connector pad on the lid being electrically connected to the signal connector pad located upon the upper surface of the die,

the bonding strip located upon the upper surface of the die being bonded by a bonding material to the bonding strip located upon the lower surface of the lid, the lid covering the electronic device but not being in physical contact with the acoustically active portion of the electronic device,

wherein the bonding strip on the upper surface of the die and the bonding strip of the lid are electrically conductive, the lid further including a conducting strip on the upper surface of the lid that is electrically connected to the bonding strip on the lower surface of the lid.

The package of claim 11 in which the bonding strip on the upper surface of the die and the bonding strip on the lower

surface of the lid completely surround the acoustically active portion of the electronic device and are bonded together so as to seal the electronic device hermetically.

ABSTRACT OF THE INVENTION

A chip-scale sized package for acoustic wave devices, acoustic resonators and similar acoustic devices located upon, or fabricated upon, or as part of, a die. The package includes a lid that is bonded to the die by a strip of solder or other bonding material so as to leave a space between the lid and that portion of the die that acoustically deforms or vibrates. The upper surface of the lid includes electrical connectors that are electrically connected via plated through holes or other means to electrical connectors, or pads on the lower surface of the lid, which pads, in turn, are electrically connected by solder or other electrically conducting material to electrical connectors to the device that are located upon the surface of the die.

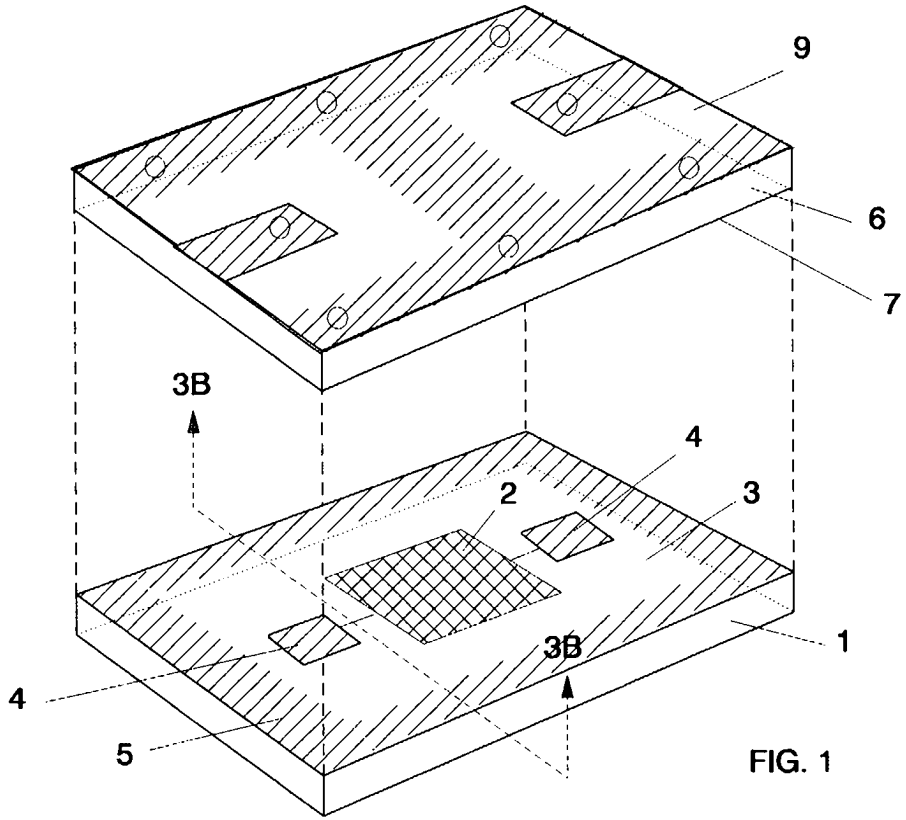

FIG. 1

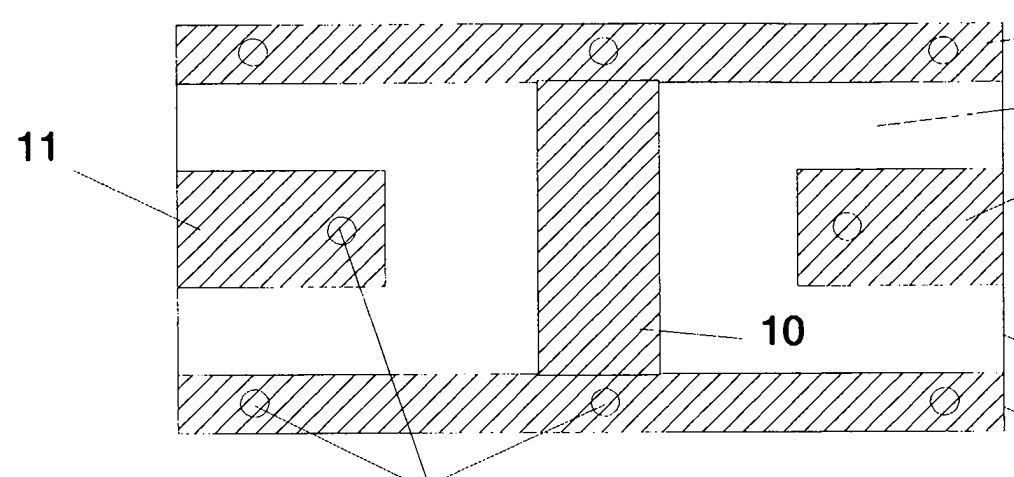

FIG. 2A

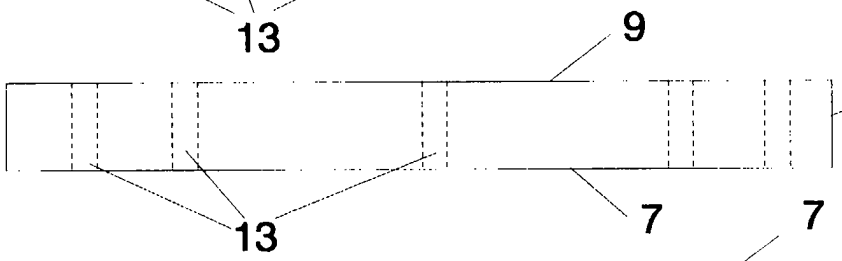

FIG. 2B

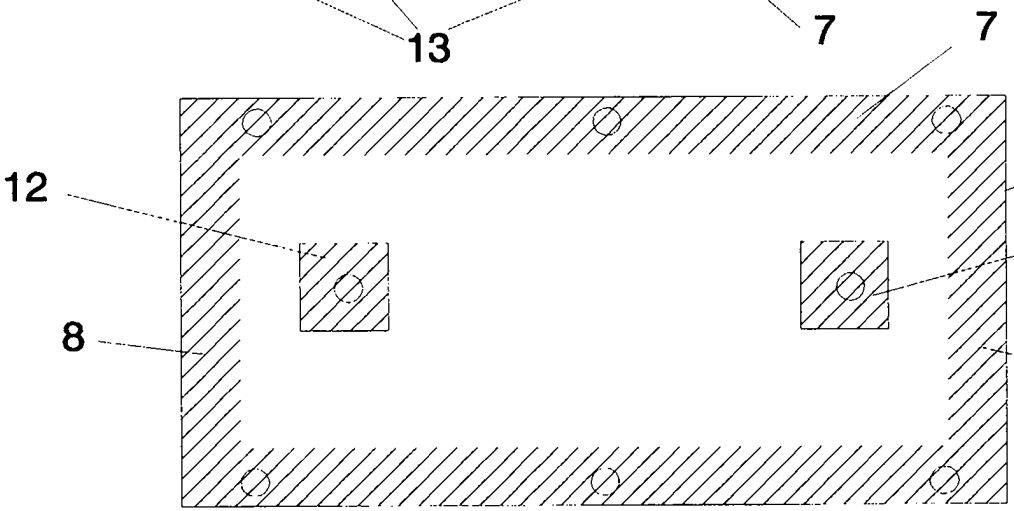

FIG. 2C

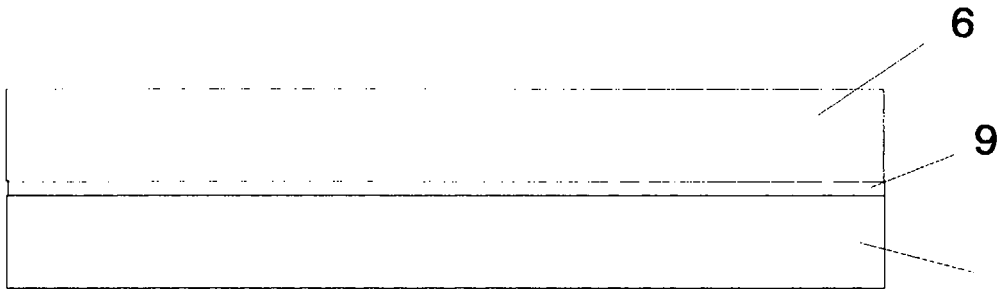

FIG. 3A

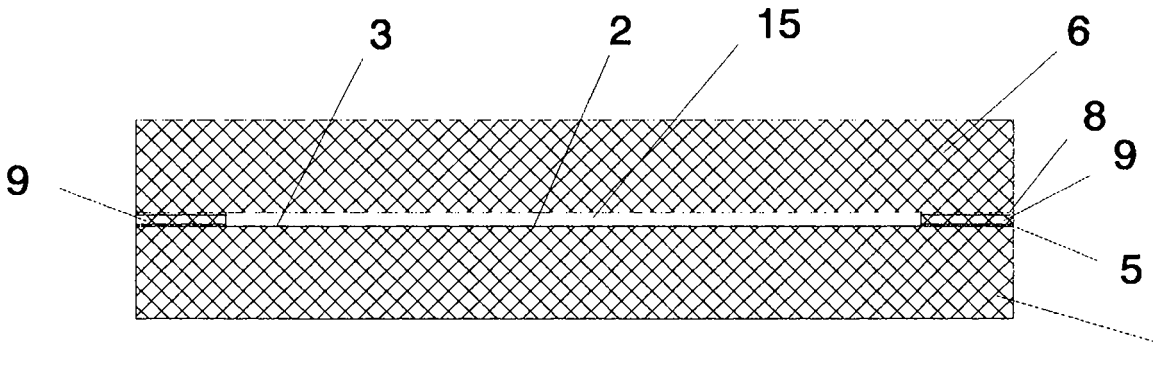

FIG. 3B

Please type a plus sign (+) inside this box → [#]

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	
First Named Inventor	Lakin
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CHIP-SCALE ELECTRONIC COMPONENT PACKAGE

(Title of the Invention)

the specification of which
☒ is attached hereto
OR
☐ was filed on (MM/DD/YYYY) _____ as United States Application Number or PCT International Application Number _____ and was amended on (MM/DD/YYYY) _____ (If applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Please type a plus sign (+) inside this box → [#]

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → Place Customer Number Bar Code Label here

OR

☒ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
G. Joseph Buck	29,519		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] OR ☒ Correspondence address below

Name	G. Joseph Buck				
Address	3868 Carson St., Ste. 315				
Address					
City	Torrance	State	CA	ZIP	90503
Country	USA	Telephone	(310) 540-8840	Fax	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Kenneth Meade	Lakin

Inventor's Signature	X Kenneth Meade Lakin					Date	X 7/10/98
Residence: City	Redmond	State	OR	Country	USA	Citizenship	USA
Post Office Address	TFR Technologies, Inc.						
Post Office Address	63140 Britta St., Ste. C-106						
City	Bend	State	OR	ZIP	97701	Country	USA

☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

Please type a plus sign (+) inside this box → [#]

PTO/SB/02A (3-97)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	**Family Name or Surname**						
Ralph Edward	Rose						
Inventor's Signature	X Ralph Edward Rose					**Date**	7-13-98
Residence: City	Bend	**State**	OR	**Country**	USA	**Citizenship**	USA
Post Office Address	TFR Technologies, Inc.						
Post Office Address	63140 Britta St., Ste. C-106						
City	Bend	**State**	OR	**ZIP**	97701	**Country**	USA

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	**Family Name or Surname**						
Kevin Thomas	McCarron						
Inventor's Signature	X					**Date**	7-10-98
Residence: City	Bend	**State**	OR	**Country**	USA	**Citizenship**	USA
Post Office Address	TFR Technologies, Inc.						
Post Office Address	63140 Britta St., Ste. C-106						
City	Bend	**State**	OR	**ZIP**	97701	**Country**	USA

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])	**Family Name or Surname**						
Inventor's Signature						**Date**	
Residence: City		**State**		**Country**		**Citizenship**	
Post Office Address							
Post Office Address							
City		**State**		**ZIP**		**Country**	

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

PTO/SB/96 (12-97)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

CERTIFICATE UNDER 37 CFR 3.73(b)

Applicant: TFR Technologies, Inc., assignee

Application No.: _____ Filed: _____

Entitled: CHIP-SCALE ELECTRONIC COMPONENT PACKAGE

TFR Technologies, Inc., a corporation,
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

certifies that it is:

1. [XX] the assignee of the entire right, title, and interest; or
2. [ ] an assignee of an undivided part interest

in the patent application identified above by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[X] Copies of assignments or other documents in the chain of title are attached.

The undersigned (whose title is supplied below) is empowered to sign this certificate on behalf of the assignee.

X July 10, 1998
Date

X _____
Signature

Kenneth M. Lakin
Typed or printed name

President
Title

PTO/SB/09 (12-97)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(b))--INDEPENDENT INVENTOR

Docket Number (Optional)

Applicant, Patentee, or Identifier: Inventor

Application or Patent No.:

Filed or Issued:

Title: CHIP-SCALE ELECTRONIC COMPONENT PACKAGE

As a below named inventor, I hereby state that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees to the Patent and Trademark Office described in:

- [x] the specification filed herewith with title as listed above.
- [ ] the application identified above.
- [ ] the patent identified above.

I have not assigned, granted, conveyed, or licensed, and am under no obligation under contract or law to assign, grant, convey, or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- [ ] No such person, concern, or organization exists.
- [x] Each such person, concern, or organization is listed below.

TFR Technologies Inc.

Separate statements are required from each named person, concern, or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

Kenneth Meade Lakin	Ralph Edward Rose	Kevin Thomas McCarron
NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
x Kenneth Meade Lakin	x Ralph Edward Rose	x Kevin Thomas McCarron
Signature of inventor	Signature of inventor	Signature of inventor
x 7/10/98	x 7-13-98	x 7-10-98
Date	Date	Date

PTO/SB/10 (12-97)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONCERN

Docket Number (Optional)

Applicant, Patentee, or Identifier: Applicant as assignee
Application or Patent No.:
Filed or Issued:
Title: CHIP-SCALE ELECTRONIC COMPONENT PACKAGE

I hereby state that I am
- ☐ the owner of the small business concern identified below:
- ☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN TFR Technologies, Inc.

ADDRESS OF SMALL BUSINESS CONCERN 63140 Britta St., Ste. C-106
Bend, Oregon, 97701

I hereby state that the above identified small business concern qualifies as a small business concern as defined in 13 CFR Part 121 for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby state that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

- ☒ the specification filed herewith with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:
- ☒ no such person, concern, or organization exists.
- ☐ each such person, concern, or organization is listed below.

Separate statements are required from each named person, concern or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

NAME OF PERSON SIGNING Kenneth Meade Lakin

TITLE OF PERSON IF OTHER THAN OWNER President

ADDRESS OF PERSON SIGNING TFR Technologies, Inc., 63140 Britta St., Ste. C-106, Bend, Oregon 97701

SIGNATURE X Kenneth Meade Lakin DATE X 7/10/98